**DAILY ASSESSMENT FORMAT**

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| **Date:** | **28/05/2020** | **Name:** | **PREETHAM S RAI** |
| **Course:** | **Logic Design** | **USN:** | **4AL18EC040** |
| **Topic:** | **Analysis of clocked sequential circuits**  **Digital clock design** | **Semester & Section:** | **4th sem ‘A’ section.** |
| **Github Repository:** | **Psraipreetham** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Topics 1**  **Clocked sequential circuits**  **The input that set flip flop to 1 is preset and the input that clears the flip flop is called direct reset.**  **The analysis of sequential circuit contains table,diagram of time sequence of input and their outputs**  **The behaviour of clocked sequential circuits are obtained from their input output and their states**  **The time sequence of input outputs and states can be enumerated by transition table**  **A seuential circuit with m flip flops and n inputs need 2m+n rows in state table**  **input equation of D flip flop is DA=A EXOR X EXOR Y**  **state table has 1 column for present state of FF**  **2 column teo inputs**  **1 column for next state of FF**  **the next state equation is A(t+1)=A EXOR X EXOR Y** |

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| **Github Repository:** |  | | |  |  | |

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